

ABSTRACT OF THE DISCLOSURE

Sub
AB

5 A data processing system is provided with a digital signal processor that has a set of instructions for intermingling byte fields selected from a selected pair of source operands and storing the ordered result in a selected destination register. A first 32-bit operand (600) is treated as four 8-bit fields while a second 32-bit operand (602) is treated as four 8-bit fields. Intermingling circuitry 702 is operable to form an ordered result in
10 accordance with each one of the set of byte intermingling instructions. An instruction is provided that performs a shift right and byte merge operation. Another instruction is provided that performs a shift left and byte merge operation. Another instruction is provided that perform a byte swap operation. A set of instructions are provided that perform various byte
15 packing and unpacking operations.

Figure 6A-6L

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